IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: **THOMAS EUGENE WACHURA** SERIAL NUMBER: **09/996,342** FILED: **NOVEMBER 21, 2001** FOR: **APPARATUS AND METHOD FOR SAMPLING EYE DIAGRAMS WITH WINDOW COMPARATORS**	PATENT ART UNIT NO.: **2863** EXAMINER: **TUNG S. LAU** ATTY DOCKET NO.: **WASC1821**

Corral de Tierra, CA
January 20, 2006

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Dear Sir:

Transmitted herewith is Response A in the above-identified application.

_X_ Small entity status of this application under 37 CFR §1.9 and §1.27 has been established by a verified statement previously submitted.

____ A verified statement to establish small entity status under 37 CFR §1.9 and §1.27 is enclosed.

TRANSMITTAL OF APPEAL BRIEF **January 20, 2006**
ATTORNEY DOCKET NO.: WASC1821

__X__ Appeal Brief and Pending Claims.

__X__ Appeal fees of $250.00 is also enclosed with PTO form 2038.

Respectfully submitted,

PENINSULA IP GROUP
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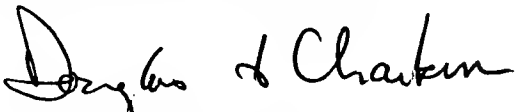

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	PATENT
THOMAS EUGENE WACHURA	ART UNIT NO.: **2863**
SERIAL NUMBER: **09/996,342**	
FILED: **NOVEMBER 21, 2001**	EXAMINER: **TUNG S. LAU**
FOR: **APPARATUS AND METHOD FOR SAMPLING EYE DIAGRAMS WITH WINDOW COMPARATORS**	Attorney Docket No.: WASC1821

Corral de Tierra, CA
January 19, 2006

CERTIFICATE OF MAILING
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Douglas A. Chaikin
Registration No. 29,140

APPEAL BRIEF

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Dear Sirs:

Appellant, in the above-noted patent application, is appealing the final rejection of Claims 1-15 made in the Examiner's Action dated July 20, 2005. The subject matter of all of the above claims having been at least twice rejected, this case is in condition for appeal to the Board in accordance with 35 U.S.C. 134.

This Appeal Brief is filed in triplicate. A check in the amount of $760.00 is included to cover the following: the fee of $510.00 for a three-month extension of time for responding to the above-noted Examiner's Action; and the fee of $250.00 for filing an appeal brief.

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02 FC:2253 510.00 OP

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I. STATUS OF CLAIMS

Claims 1-16 are pending and stand rejected in the instant application. Claims 1-16 are hereby appealed. For ease of reference and consideration, a copy of the claims involved in this appeal is attached hereto as Appendix A.

II. STATUS OF THE AMENDMENTS

The instant application was filed on November 21, 2001. In response to a Final Rejection dated June 7, 2004, Claims 1 and 15 were amended to clarify the specific structural and functional features of the invention. The Examiner has maintained his rejection of the pending claims, including Claims 1 and 15, as amended. Therefore, no claim pending in the instant application has been amended subsequent to the Final Rejection dated June 7, 2004.

III. SUMMARY OF THE INVENTION

The instant invention is directed to an apparatus and corresponding method for measuring the characteristics of a bit stream of binary pulses (paragraphs 18-20). The measuring of the bit stream characteristics is performed by a window comparator which samples an input signal of bit stream pulses, and determines whether the voltage characteristic (e.g. voltage magnitude) of the bit stream pulses is within a voltage threshold window, which is capable of moving between several voltages during various times of the input signal frequency. As illustrated in FIG. 2 and described, for example, in paragraph 20, lines 1-5 and 11-15 the voltage threshold window is generated by a control apparatus that:

> "...applies a value of voltage V + ΔV 200 to the plus input of comparator 202 and a value of V, 201, to the minus input of comparator 203 to crate a voltage threshold window..."

Subsequently, logic means (e.g. an accumulator) counts the number of bit stream pulses having voltage characteristics that fall within the voltage threshold window (see, paragraph 21). Thus, the instant invention discloses and claims an apparatus including:

"...control means for defining a window comparator..."

that includes a bounded voltage threshold window defining a minimum and maximum voltage magnitude of interest for a given bit stream period and

"...logic means for accumulating the time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during durations of the binary pulse bit stream..."

IV. ISSUES PRESENTED ON APPEAL

A. Whether the Examiner improperly rejected Claims 1-6 under 35 U.S.C. §102.

B. Whether the invention defined by Claims 1-6 is anticipated by the cited reference.

C. Whether the Examiner improperly rejected Claims 7-8 under 35 U.S.C. §102.

D. Whether the invention defined by Claims 7-8 is anticipated by the cited reference.

E. Whether the Examiner improperly rejected Claims 9-14 under 35 U.S.C. §102.

F. Whether the invention defined by Claims 9-14 is anticipated by the cited reference.

G. Whether the Examiner improperly rejected Claims 15-16 under 35 U.S.C. §102.

H. Whether the invention defined by Claims 15-16 is anticipated by the cited reference.

V. GROUPING OF CLAIMS

For purposes of this Appeal, the pending claims shall be grouped as follows:

Group 1: Claims 1-6 directed to an apparatus for measuring characteristics of a bit stream of binary pulses;

Group 2: Claims 7-8 directed to an apparatus for measuring characteristics of a bit stream of binary pulses;

Group 3: Claims 9-14 directed to a method for determining characteristics of a bit stream of binary pulses; and

Group 4: Claims 15-16 directed to a method for determining characteristics of a bit stream of binary pulses.

VI. ARGUMENT

A. Claims 1-6 have been improperly rejected as the cited reference does not include each and every limitation of the pending claims

For a claim to be properly rejected under 35 U.S.C. 102, "...each and every element as set forth in the claims [must be] found either expressly or inherently described, in a single prior art reference..." MPEP 2131, *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996), *Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc.*, 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). During the prosecution of the instant application, the Examiner has not provided a one-to-one correspondence to at least one limitation of the above-noted claims or otherwise has misunderstood the claimed invention. For example, in rejecting Claim 1, the Examiner stated in the January 12, 2005 Office Action (and reiterated the same in the Final Office Action) that:

> "...Thomas Eugene, James Roger, Robert Lee disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator (abstract, fig. 2, unit 203, 200), and logic means for accumulating time and voltage event counts (Col. 4-6, section 0017-0019) of the bit stream pulses falling within voltage threshold and points inside the window comparator during durations of the binary bit stream and drawing eye diagrams there from defining the bit stream characteristics..."

Thus, as understood from the above characterization of elements, the Examiner is asserting that the count logic of Waschura, et al. is the same as the "...window comparator..." limitation of claim 1. Such assertion is contrary to the disclosure of Waschura, et al. that must be considered when rejecting the pending claims. MPEP2131. As illustrated, for example, in FIG. 2 and as described, for example, in paragraph 19, lines 1-2:

> "...Count logic 20 has a one-bit comparator 200 with one input connected to the transmission facility 12 or other point in the transmitter 10 or receiver 11 to measure the high speed binary coded bit stream..."

And as further disclosed in paragraph 19, lines 5-8:

> "...the one-bit comparator 200 will output a high when the signal voltage on the positive pin is higher than the signal voltage on the negative pin..."

Thus, Waschura, et al. discloses a single threshold value element that outputs a logical one when the input signal voltage is greater than a threshold value. The single (e.g. threshold) value cannot and does not behave as a window or two-value element as provided in Claim 1, as the disclosure appears to be silent on such an element.

In contrast, the "...window comparator..." of Claim 1 is illustrated in Fig. 2 and described, for example, in paragraph 20, lines 11-15 as being a control apparatus that:

> "...applies a value of voltage V+ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the window as recited in Claim 1 is defined as being bounded by two values: an upper voltage value V+ΔV; and a lower voltage value of V. Thus, the claimed window comparator of the instant application defines a voltage window area defined by upper and lower limits. The single value comparator (e.g. comparator 200) of Waschura, et al. does not correspond to the window comparator of Claim 1. Thus, at least the following limitation of Claim 1 is not disclosed in Waschura, et al.- "...control means for defining a widow comparator..."

In corresponding fashion, the count logic (e.g. threshold counter 203) of Waschura, et al. does not correspond to the count logic of Claim 1 in that the count logic of Waschura, et al. does not:

> "...accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during duration of the binary pulse bit stream..."

as the circuit described in Waschura, et al. is not capable of defining a voltage window; thus, it is not capable of counting instances of a voltage being within

voltage thresholds. As disclosed, for example, in paragraph 17, lines 1-3 and 8-11:

> "...count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses on the binary coded pulse bit stream..."

Thus, Waschura, et al. discloses sampling and accumulating voltage values that exceed a given threshold value; not sampling and accumulating voltage values that "...fall within voltage thresholds and points inside the window comparator..." as defined in Claim 1. Accordingly, at least this limitation is not disclosed within Waschura, et al. Consequently, as neither of the aforementioned limitations are disclosed in Waschura, the rejection of Claim 1 under 35 U.S.C. 102 is improper and should be withdrawn.

Claims 2-6 directly or indirectly depend from and incorporate all of the limitations thereof. For the foregoing reasons set forth with respect to Claim 1, it is submitted that the rejection of Claims 2-6 under 35 U.S.C. 102 is also improper and should be withdrawn.

B. Claims 1-6 are not anticipated by the cited reference as Waschura, et al does not disclose each and every limitation of the pending claims

Notwithstanding the Examiner's improper rejection of Claims 1-6, such claims are also not anticipated by the cited reference as Waschura, et al. does not include, for example:

> "...control means for defining a window comparator..." and

> "...logic means for accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during durations of the binary pulse bit stream..."

as defined in Claim 1. Consequently, Waschura, et al. does not anticipate the invention as defined in Claim 1.

As understood, and disclosed, for example, in paragraph 17, Waschura, et al. is directed to an apparatus that measures the voltage characteristics of an input signal, for example, by generating one or more maximum threshold voltage levels (see, paragraph 12) and sampling and accumulating the number of times the sampled input signal voltage exceeds the maximum voltage threshold voltage. Waschura, et al. operates by: (1) establishing an upper voltage threshold level; (2) sampling an input signal to determine if the sampled voltage level exceeds the voltage threshold; and (3) if the sampled voltage value exceeds the maximum voltage threshold value, then and accumulator circuitry is accumulated. There is no discussion present within Waschura, et al. of generating a minimum voltage threshold value; therefore, Waschura, et al. is silent on generating a window comparator, including a minimum and a maximum value. Voltage steps are mentioned, for example, in paragraph 17, but such voltage steps are added to the previous voltage (see, paragraph 17, lines 13-19) to generate a larger threshold voltage; not providing a lower voltage bound.

In contradistinction, the instant invention, as defined in Claim 1, recites defining a window comparator as being a control apparatus that:

> "...applies a value of voltage V+ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the window comparator as recited in Claim 1 is defined as being bounded by two values: an upper voltage value V+ΔV; and a lower voltage value of V. Thus, the claimed window comparator of the instant application defines a voltage window area defined by upper and lower limits. The single value comparator (e.g. comparator 200) of Waschura, et al. does not correspond to the window comparator of Claim 1. Thus, at least the "...control means for defining a window comparator..." limitation is not disclosed in Waschura, et al.

In corresponding fashion, Waschura, et al. does not disclose the limitation of:

> "...accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during duration of the binary pulse bit stream..."

as recited in Claim 1 as the circuit described in Waschura, et al. is not capable of defining a voltage window; thus, it is not capable of counting instances of a voltage being within voltage thresholds. As disclosed, for example, in paragraph 17, lines 1-3 and 8-11:

> "...count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses on the binary coded pulse bit stream..."

Thus, Waschura, et al. discloses sampling and accumulating voltage values that exceed a given threshold value; not sampling and accumulating voltage values that "...fall within voltage thresholds and points inside the window comparator..." as defined in Claim 1. Accordingly, at least this limitation is not disclosed within Waschura, et al. Consequently, as neither of the aforementioned limitations are disclosed in Waschura, the rejection of Claim 1 under 35 U.S.C. 102 is improper and should be withdrawn.

Claims 2-6 directly or indirectly depend from and incorporate all of the limitations thereof. For the foregoing reasons set forth with respect to Claim 1, it is submitted that the rejection of Claims 2-6 under 35 U.S.C. 102 is also improper and should be withdrawn.

C. Claims 7-8 have been improperly rejected as the cited reference does not include each and every limitation of the pending claims

As discussed above, for a claim to be properly rejected under 35 U.S.C. 102, "...each and every element as set forth in the claims [must be] found either expressly or inherently described, in a single prior art reference..." MPEP 2131, *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996), *Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc.*, 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). During the

prosecution of the instant application, the Examiner has not provided a one-to-one correspondence to at least one limitation of the above-noted claims or otherwise has misunderstood the claimed invention. For example, in rejecting Claim 7, the Examiner stated in the January 12, 2005 Office Action (and reiterated the same in the Final Office Action) that:

> "...Thomas Eugene, James Roger, Robert Lee disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator of an array of columns and rows defining points for accumulating voltage counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream (abstract, fig. 2, unit 203, 200), and apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels (Col. 4-6, section 0017-0019, fig. 3, unit 21111, fig. 4, unit 21120) with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 2, 203, 200, 214, fig. 3, unit 21113-21117, fig. 5, 6)..."

Thus, as understood from the above characterization of elements, the Examiner is asserting that the count logic of Waschura, et al. is the same as the "...window comparator..." limitation of Claim 7. Such assertion is contrary to the disclosure of Waschura, et al. that must be considered when rejecting the pending claims. MPEP2131. As illustrated, for example, in FIG. 2 and as described, for example, in paragraph 19, lines 1-2:

> "...Count logic 20 has a one-bit comparator 200 with one input connected to the transmission facility 12 or other point in the transmitter 10 or receiver 11 to measure the high speed binary coded bit stream..."

And as further disclosed in paragraph 19, lines 5-8:

> "...the one-bit comparator 200 will output a high when the signal voltage on the positive pin is higher than the signal voltage on the negative pin..."

Thus, Waschura, et al. discloses a single threshold value element that outputs a logical one when the input signal voltage is greater than a threshold value. The single (e.g. threshold) value cannot and does not behave as a window or two-value element as provided in Claim 7, as the disclosure appears to be silent on such an element.

In contrast, the "...window comparator..." of Claim 7 is illustrated in Fig. 2 and described, for example, in paragraph 20, lines 11-15 as being a control apparatus that:

> "...applies a value of voltage V+ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the window as recited in Claim 7 is defined as being bounded by two values: an upper voltage value V+ΔV; and a lower voltage value of V. Thus, the claimed window comparator of the instant application defines a voltage window area defined by upper and lower limits. The single value comparator (e.g. comparator 200) of Waschura, et al. does not correspond to the window comparator of Claim 7. Thus, at least the following limitation of Claim 7 is not disclosed in Waschura, et al.- "...control means for defining a widow comparator..."

In corresponding fashion, the count logic (e.g. threshold counter 203) of Waschura, et al. does not correspond to the voltage threshold window and count logic limitations of Claim 7 in that Waschura, et al. is silent on:

> "...accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during duration of the binary pulse bit stream..."

as the circuit described in Waschura, et al. is not capable of defining a voltage window; thus, it is not capable of counting instances of a voltage being within voltage thresholds. As disclosed, for example, in paragraph 17, lines 1-3 and 8-11:

> "...count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses on the binary coded pulse bit stream..."

Thus, Waschura, et al. discloses sampling and accumulating voltage values that exceed a given threshold value, not:

> "...apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels...and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window..."

as defined in Claim 7. Accordingly, at least this limitation is not disclosed within Waschura, et al. Consequently, as neither of the aforementioned limitations are disclosed in Waschura, the rejection of Claim 7 under 35 U.S.C. 102 is improper and should be withdrawn.

With respect to Claim 8, the Examiner has maintained his rejection of such claim by asserting that the single element comparator (fig. 200) and the above threshold counter (203) of Waschura et al. are equivalent to the following elements:

> "....first control means for defining a window comparator..."
>
> "...second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array..." and
>
> "...first counter means for accumulating counts of the detected binary pulse voltage levels at time offsets during each defined duration time of the binary pulse bit stream in a column and row point of the array..."

However, as discussed in greater detail above, Waschura, et al. is silent on creating a voltage threshold window that moves between a minimum and maximum voltage threshold. Waschura, et al. is directed to and discloses a single value comparator (FIG. 2, element 200) that is capable of determine whether an input signal value exceeds a reference value; it is not capable of determining whether the input signal value is less than a lower bound, not is

there an element within Waschura, et al. capable of generating and making lower bound determinations. Thus, as Waschura, et al. is silent on an element capable of functioning as a lower bound and containing circuitry operable to determine whether an input signal is less than such lower bound, Waschura, et al. at least does not disclose "...second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold..." as defined in Claim 8.

In corresponding fashion, Waschura, et al. also does not disclose "...logic means for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold..." as no voltage threshold window is created by the apparatus of Waschura, et al. Consequently, at least this limitation of Claim 8 is not disclosed by Waschura, et al. Accordingly, the rejection of Claims 7-8 is improper and should be withdrawn.

D. Claims 7-8 are not anticipated by the cited reference as Waschura, et al. does not disclose each and every limitation of the pending claims

Notwithstanding the Examiner's improper rejection of Claims 7-8, such claims are also not anticipated by the cited reference as Waschura, et al. does not disclose, for example:

> "...control means for defining a window comparator..." and
>
> "...apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage level with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring a time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window ..."

as defined in Claim 7 and, for example:

> "...first control means for defining a window comparator..." and

> "...second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array..." and
>
> "...logic means for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold..."

as defined in Claim 8. Consequently, Waschura, et al. does not anticipate the invention as defined in Claims 7-8.

As understood, and disclosed, for example, in paragraph 17, Waschura, et al. is directed to an apparatus that measures the voltage characteristics of an input signal, for example, by generating one or more maximum threshold voltage levels (see, paragraph 12) and sampling and accumulating the number of times the sampled input signal voltage exceeds the maximum voltage threshold voltage. Waschura, et al. operates by: (1) establishing an upper voltage threshold level; (2) sampling an input signal to determine if the sampled voltage level exceeds the voltage threshold; and (3) if the sampled voltage value exceeds the maximum voltage threshold value, then and accumulator circuitry is accumulated. There is no discussion present within Waschura, et al. of generating a minimum voltage threshold value; therefore, Waschura, et al. is silent on generating a window comparator, including a minimum and a maximum value. Voltage steps are mentioned, for example, in paragraph 17, but such voltage steps are added to the previous voltage (see, paragraph 17, lines 13-19) to generate a larger threshold voltage; not providing a lower voltage bound.

In contradistinction, the instant invention, as defined in Claim 1, recites defining a window comparator as being a control apparatus that:

> "...applies a value of voltage V+ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the window comparator as recited in Claims 7-8 is defined as being bounded by two values: an upper voltage value V+ΔV; and a lower voltage value of V. Thus, the claimed window comparator of the instant application defines a

voltage window area defined by upper and lower limits. The single value comparator (e.g. comparator 200) of Waschura, et al. does not correspond to the window comparator of Claims 7-8. Thus, at least the "...control means for defining a window comparator..." limitation as defined in Claims 7-8 and the "...second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold..." as defined in Claim 8 is not disclosed in Waschura, et al.

In corresponding fashion, Waschura, et al. does not disclose the limitation of:

> "...accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during duration of the binary pulse bit stream..."

as recited in Claim 7 as the circuit described in Waschura, et al. is not capable of defining a voltage window; thus, it is not capable of counting instances of a voltage being within voltage thresholds. As disclosed, for example, in paragraph 17, lines 1-3 and 8-11:

> "...count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses on the binary coded pulse bit stream..."

Thus, Waschura, et al. discloses sampling and accumulating voltage values that exceed a given threshold value; not sampling and accumulating voltage values that "...fall within voltage thresholds and points inside the window comparator..." as defined in Claim 7. Accordingly, at least this limitation is not disclosed within Waschura, et al. Consequently, as neither of the aforementioned limitations are disclosed in Waschura, the rejection of Claims 7-8 under 35 U.S.C. 102 is improper and should be withdrawn.

E. <u>Claims 9-14 have been improperly rejected as the cited reference does not include each and every limitation of the pending claims</u>

As discussed above, for a claim to be properly rejected under 35 U.S.C. 102, "...each and every element as set forth in the claims [must be] found either expressly or inherently described, in a single prior art reference..." MPEP 2131, *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996), *Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc.*, 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). During the prosecution of the instant application, the Examiner has not provided a one-to-one correspondence to at least one limitation of the above-noted claims or otherwise has misunderstood the claimed invention. For example, in rejecting Claim 9, the Examiner stated in the January 12, 2005 Office Action (and reiterated the same in the Final Office Action) that:

> "...Thomas Eugene, James Roger, Robert Lee disclose a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator, and accumulating various voltage counts (Col. 4-6, section 0017-0019, fig. 3, unit 21113, 2114-21117) of the bit stream pulses at time offsets defined duration times of the binary pulse bit stream within voltage threshold at points inside the window comparator and drawing an eye diagram there from defining the bit stream pulse characteristics (fig. 2, 203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6, Col. 4-6, section 0017-0019)..."

Thus, as understood from the above characterization of elements, the Examiner is asserting that the operation of the count logic of Waschura, et al. is the same as the "...defining a window comparator..." step of Claim 9. Such assertion is contrary to the disclosure of Waschura, et al. that must be considered when rejecting the pending claims. MPEP2131. As disclosed, for example, in paragraph 21, lines 9-14, Waschura, et al. operates by initially setting the threshold value to a minimum value from which a subsequent sample is taken. During the next pass, "...the variable voltage threshold VVT is increased by the value of the voltage step, V..." from which a subsequent sample is taken at a later time.

And as further disclosed in paragraph 19, lines 5-8:

> "...the one-bit comparator 200 will output a high when the signal voltage on the positive pin is higher than the signal voltage on the negative pin..."

Thus, Waschura, et al. discloses a single threshold value element that outputs a logical one when the input signal voltage is greater than a threshold value, which is incrementally modified upwards. The single (e.g. threshold) value cannot and does not behave as a window or two-value element as provided in Claim 9, as the disclosure appears to be silent on such an element.

In contrast, the step of "...defining a window comparator..." of Claim 9 is illustrated in Fig. 2 and described, for example, in paragraph 20, lines 11-15 as being provided by a control apparatus that:

> "...applies a value of voltage V+ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the window as recited in Claim 9 is defined as being bounded by two values: an upper voltage value V+ΔV; and a lower voltage value of V. Thus, the claimed window comparator definition of the instant application relates to a voltage window area defined by upper and lower limits. The incremental, single value voltage threshold generation steps of Waschura, et al. does not correspond to the defining a window comparator step of Claim 9. Thus, at least the aforementioned limitation of Claim 9 is not disclosed in Waschura, et al.

In corresponding fashion, the step of:

> "...accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during duration of the binary pulse bit stream..."

is also not disclosed in Waschura, et al. as the circuit described in Waschura, et al. is not capable of defining a voltage window; it only increments a previous value. Thus, it is not capable of counting instances of a voltage being within voltage thresholds. As disclosed, for example, in paragraph 17, lines 1-3 and 8-11:

> "...count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses on the binary coded pulse bit stream..."

Thus, Waschura, et al. discloses sampling and accumulating voltage values that exceed a given threshold value; not:

> "...accumulating various voltage counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage thresholds at points inside the window comparator ..."

as defined in Claim 9. Accordingly, at least the aforementioned limitation of Claim 9 is not disclosed within Waschura, et al. Consequently, as neither of the aforementioned limitations are disclosed in Waschura, the rejection of Claim 9 under 35 U.S.C. 102 is improper and should be withdrawn.

Claims 10-14 directly or indirectly depend from and incorporate all of the limitations thereof. For the foregoing reasons set forth with above respect to Claim 9, it is submitted that the rejection of Claims 10-14 under 35 U.S.C. 102 is also improper and should be withdrawn.

F. Claims 9-14 are not anticipated by the cited reference as Waschura, et al
does not disclose each and every limitation of the pending claims

Notwithstanding the Examiner's improper rejection of Claims 9-14, such claims are also not anticipated by the cited reference as Waschura, et al. does not include, for example, the steps of:

"...defining a window comparator..." and

"...accumulating various voltage counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage thresholds at points inside the window comparator....."

as defined in Claim 9. Consequently, Waschura, et al. does not anticipate the invention as defined in Claim 9.

As understood, and disclosed, for example, in paragraph 17, Waschura, et al. is directed to an apparatus that measures the voltage characteristics of an input signal, for example, by generating one or more maximum threshold voltage levels (see, paragraph 12) and sampling and accumulating the number of times the sampled input signal voltage exceeds the maximum voltage threshold voltage. Waschura, et al. operates by: (1) establishing an upper voltage threshold level; (2) sampling an input signal to determine if the sampled voltage level exceeds the voltage threshold; (3) if the sampled voltage value exceeds the maximum voltage threshold value, increment the accumulated value; and (4) during a subsequent time period, increase the threshold value by a given voltage step (paragraph 21, lines 9-14); and (5) increment the accumulated value if the sampled voltage vale exceeds the incremented voltage threshold There is no discussion present within Waschura, et al. of generating a minimum voltage threshold value; therefore, Waschura, et al. is silent on defining a window comparator, including a minimum and a maximum value.

In contradistinction, the invention as defined in Claim 1, recites defining a window comparator as a circuit performing the following steps:

> "...applies a value of voltage V+ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the defined window comparator of Claim 9 is bounded by two values: an upper voltage value V+ΔV; and a lower voltage value of V. The single value comparator operation of Waschura, et al. does not correspond to the window comparator definition step of Claim 9. Thus, at least the "...defining a window comparator..." step of Claim 9 is not disclosed in Waschura, et al.

In corresponding fashion, Waschura, et al. also does not disclose the step of:

> "...accumulating various voltage counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage thresholds at points inside the window comparator..."

as recited in Claim 9 as the circuit described in Waschura, et al. is not capable of defining a voltage window; thus, it is not capable of accumulating voltage counts of the bit stream...within voltage thresholds at points inside the window comparator..." As disclosed, for example, in paragraph 17, lines 1-3 and 8-11:

> "...count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses on the binary coded pulse bit stream..."

Thus, Waschura, et al. discloses sampling and accumulating voltage values that exceed a single threshold value; not sampling and accumulating voltage values that "...fall within voltage thresholds and points inside the window comparator..." as defined in Claim 9. Accordingly, the aforementioned limitation is not disclosed within Waschura, et al. Consequently, as neither of the aforementioned limitations are disclosed in Waschura, the rejection of Claim 9 under 35 U.S.C. 102 is improper and should be withdrawn.

Claims 10-14 directly or indirectly depend from and incorporate all of the limitations thereof. For the foregoing reasons set forth above with respect to

Claim 9, it is submitted that the rejection of Claims 10-14 under 35 U.S.C. 102 is also improper and should be withdrawn.

G. Claims 15-16 have been improperly rejected as the cited reference does not include each and every limitation of the pending claims

For a claim to be properly rejected under 35 U.S.C. 102, "...each and every element as set forth in the claims [must be] found either expressly or inherently described, in a single prior art reference..." MPEP 2131, *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996), *Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc.*, 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). During the prosecution of the instant application, the Examiner has not provided a one-to-one correspondence to at least one limitation of the above-noted claims or otherwise has misunderstood the claimed invention. For example, in rejecting Claims 15-16, the Examiner stated (page 13) in the January 12, 2005 Office Action (and reiterated the same in the Final Office Action) that:

> "...Thomas Eugene, James Roger, Robert Lee disclose a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream, creating a voltage threshold window that moves between defined voltage levels at each row of the array, detecting voltage levels of the binary of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array, accumulating counts of the detected binary pulse voltage levels at the time offsets in a column and row point of the array..."
>
> and further stated that:
>
> "...the examiner reminds to the applicants that during patent examination, the pending claims must be given the broadest reasonable interpretation consistent with the specification..."

and then proceeds to reject the pending claims as being anticipated. However, the Examiner has not provided a pointer as to where the following limitations of Claims 15-16 are disclosed in Waschura, et al.:

> "...creating a voltage threshold window that moves between a minimum voltage and a maximum voltage..." and
>
> "...accumulating counts of voltage levels of the binary pulses occurring at time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window..."

and the following limitation of Claim 16:

> "...detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window..."

as Waschura, et al. is silent on generating or otherwise creating a comparator window including a voltage threshold window that moves between minimum voltage and a maximum voltage. As understood, and disclosed, for example, in paragraph 17, Waschura, et al. is directed to an apparatus that measures the voltage characteristics of an input signal, for example, by generating one or more maximum threshold voltage levels (see, paragraph 12) and sampling and accumulating the number of times the sampled input signal voltage exceeds the maximum voltage threshold voltage. Waschura, et al. operates by: (1) establishing an upper voltage threshold level; (2) sampling an input signal to determine if the sampled voltage level exceeds the voltage threshold; (3) if the sampled voltage value exceeds the maximum voltage threshold value, increment the accumulated value; and (4) during a subsequent time period, increase the threshold value by a given voltage step (paragraph 21, lines 9-14); and (5) increment the accumulated value if the sampled voltage vale exceeds the incremented voltage threshold There is no discussion present within Waschura, et al. of generating a minimum voltage threshold value; therefore, Waschura, et al. is silent on defining a window comparator, including a minimum and a maximum value.

Consequently, as Waschura, et al. is silent on defining a window comparator, including a minimum and a maximum value, at least the aforementioned limitation is not disclosed by Waschura, et al. Accordingly, the rejection of Claims 15-16 is improper and should be withdrawn.

H. Claims 15-16 are not anticipated by the cited reference as Waschura, et al.
does not disclose each and every limitation of the pending claims

Notwithstanding the Examiner's improper rejection of Claims 15-16, such claims are also not anticipated by the cited reference as Waschura, et al. does not perform the following steps:

"...defining a comparator window comparator..."

"...creating a voltage threshold voltage window that moves between a minimum voltage and a maximum voltage..."

as defined in Claim 15 as Waschura, et al. does not generate or otherwise define a comparator window or call for moving such voltage threshold window as Waschura, et al. discloses a single-value comparator that detects whether a input signal voltage exceeds a threshold voltage (paragraph 17). Then the threshold value is increased by a step amount (paragraph 17, lines 9-13), and then subsequently compared to the input signal value. Thus, the threshold value is increased before a subsequent comparison is made. Waschura, et al. is silent on generating a lower limit of a window to compare an input signal value to. As such, Waschura, et al. also does not disclose the following limitation of Claim 16:

"...creating a voltage threshold window that moves between defined voltage levels..." and

"...detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window..."

Consequently, Waschura, et al. does not anticipate the invention as defined in Claims 15-16. Accordingly, the rejection of Claims 15-16 is improper and should be withdrawn.

VII. CONCLUSION

Based on the foregoing arguments, it is submitted that the Examiner's rejections are in error that Claims 1-16 are not anticipated within the meaning of 35 U.S.C. 102 in view the cited reference.

Accordingly, it is respectfully submitted that the instant application is in form for allowance, and such action is earnestly solicited.

Respectfully submitted

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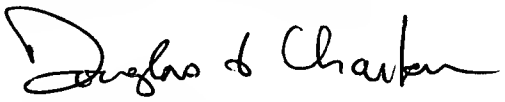

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PENDING CLAIMS

1. (Previously Presented) Apparatus for measuring characteristics of a bit stream of binary pulses comprising

control means for defining a window comparator, and

logic means for accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics.

2. (Original) The apparatus for measuring characteristics of a bit stream of binary pulses set forth in Claim 1 wherein the control means comprises:

programmable means for establishing an array of columns and rows defining the points for accumulating counts of pulse voltage levels at time offsets during the duration times and for creating a voltage threshold window that moves between a minimum and maximum voltage with changes of rows of the array.

3. (Original) The apparatus for measuring characteristics of a bit stream of binary pulses set forth in Claim 2 wherein the logic means comprises:

logic circuitry for detecting voltage levels of the binary pulses occurring at various time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array.

4. (Original) The apparatus for measuring characteristics of a bait stream of binary pulses set forth in Claim 3 wherein the logic means comprises:

first counter means for accumulating counts of the detected binary pulse voltage levels at the time offsets during each duration part of the binary pulse bit stream in a column and row point of the array.

5. (Original) The apparatus for measuring characteristics of a bit stream of binary pulses set forth in Claim 4 wherein the logic means comprises:

second counter means for defining duration times of the bit stream of binary pulses to accumulate the counts of the detected binary pulse voltage levels falling within the voltage threshold window at each point of the array.

6. (Original) The apparatus for measuring characteristics of a bit stream of binary pulses set forth in Claim 5 further comprising:

apparatus for displaying the array column and row points of accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses.

7. (Original) Apparatus for measuring characteristics of a bit stream of binary pulses comprising:

control means for defining a window comparator of an array of columns and rows defining points for accumulating voltage counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream, and

apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses.

8. (Original) Apparatus for measuring characteristics of a bit stream of binary pulses comprising:

first control means for defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream,

second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array,

logic means for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold at each row and column point of the array,

first counter means for accumulating counts of the detected binary pulse voltage levels at time offsets during each defined duration time of the binary pulse bit stream in a column and row point of the array,

second counter means for determining duration of periods of the binary bit stream in which to accumulate the detected binary pulse voltage levels at each point of the array, and

monitor apparatus for displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses.

9. (Previously Presented) A method for determining characteristics of a bit stream of binary pulses comprising the steps of

defining a window comparator, and

accumulating various voltage counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage thresholds at points inside the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics.

10. (Original) The method for determining characteristics of the bit stream of binary pulses set forth in Claim 9 wherein the window comparator defining step comprises the step of:

establishing an array of columns and rows defining the points for accumulating the event counts at time offsets during the defined duration times.

11. (Original) The method for determining characteristics of the bit stream of binary pulses set forth in Claim 10 wherein the window comparator defining step comprises the step of:

creating a voltage threshold window that moves with respect to a minimum and maximum voltage threshold wherein the voltage threshold window changes with respect to the rows of the array.

12. (Original) The method for determining characteristics of the bit stream of binary pulses set forth in Claim 11 wherein the event count accumulating step comprises the step of:

detecting voltage levels of the binary pulses occurring at the time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array.

13. (Original) The method for determining characteristics of the bit stream of binary pulses set forth in Claim 12 wherein the event count accumulating step comprises the step of:

accumulating counts of the detected binary pulse voltage levels at the time offsets during each duration part of the binary pulse bit stream in a column and row point of the array.

14. (Original) The method for determining characteristics of the bit stream of binary pulses set forth in Claim 13 wherein the event count accumulating step comprises the step of:

displaying the array column and row points of accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses.

15. (Previously Presented) A method for determining characteristics of a bit stream of binary pulses comprising the steps of:

defining a window comparator of an array of columns and rows defining points for accumulating event counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream;

creating a voltage threshold window that moves between a minimum voltage and a maximum voltage at each row of the array; and

accumulating counts of voltage levels of the binary pulses occurring at time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses.

16. (Previously Presented) A method for determining characteristics of a bit stream of binary pulses comprising the steps of:

defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream;

creating a voltage threshold window that moves between defined voltage levels at each row of the array;

detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array;

accumulating counts of the detected binary pulse voltage levels at the time offsets in a column and row point of the array; and

displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses.